

Notice of Allowability	Application No.	Applicant(s)	
	10/781,707	COLE ET AL.	
	Examiner	Art Unit	
	Ida M. Soward	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to the Applicants amendment filed August 11, 2006.
2. ☒ The allowed claim(s) is/are 1,3-24,27-46 and 69-82.
3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) ☐ All b) ☐ Some* c) ☐ None of the:
 1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

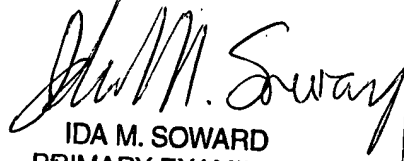
Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
 - (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
 - 1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
 - (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

- | | |
|--|--|
| <ol style="list-style-type: none"> 1. <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) 2. <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) 3. <input type="checkbox"/> Information Disclosure Statements (PTO/SB/08),
Paper No./Mail Date _____ 4. <input type="checkbox"/> Examiner's Comment Regarding Requirement for Deposit
of Biological Material | <ol style="list-style-type: none"> 5. <input type="checkbox"/> Notice of Informal Patent Application 6. <input type="checkbox"/> Interview Summary (PTO-413),
Paper No./Mail Date _____ 7. <input type="checkbox"/> Examiner's Amendment/Comment 8. <input checked="" type="checkbox"/> Examiner's Statement of Reasons for Allowance 9. <input type="checkbox"/> Other _____ |
|--|--|


 IDA M. SOWARD
 PRIMARY EXAMINER

DETAILED ACTION

This Office Action is in response to the Applicants amendment filed August 11, 2006.

Allowable Subject Matter

Claims 1, 3-24, 27-46 and 69-82 are allowed.

The following is an examiner's statement of reasons for allowance: The prior art of record does not disclose, make obvious, or otherwise suggest the structure of the applicant's together with the other limitations of the independent claims, such as:

In claim 1, "a trench structure around at least a portion of the array, wherein the trench structure extends from the surface to the lower layer, and wherein the trench structure prevents at least a portion of photons or charged particles from passing through the trench structure to the array wherein said trench structure has a top width and a base layer width and the base layer width is smaller than the top width wherein the trench structure has sidewalls and contains a first material that prevents at least a portion of photons or charged particles from passing through the trench structure to the array";

in claim 13, "a trench formed in a substrate of the integrated circuit along at least a portion of a periphery of the active area, the substrate having a lower layer and an upper layer on the lower layer, wherein the trench extends from a surface of the upper

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layer to a surface of the lower layer and the trench includes a top width and a base layer width where the base layer width is smaller than the top width; an insulating liner formed along sidewalls of the trench; and a first fill material formed over the insulating liner wherein the first fill material at least partially fills the trench and prevents at least a portion of photons and electrons from passing through the trench to the active area”;

in claim 24, “a plurality of trenches formed in a substrate of the integrated circuit on at least a portion of a periphery of the active area, wherein a depth of each of the plurality of trenches extends to a surface of a base layer of said substrate and where at least one trench of the plurality of trenches includes a top width and a base layer width where the base layer width is smaller than the top width further comprising an insulating liner formed along each sidewall of the plurality of trenches wherein the insulating liner comprises a high absorption material”;

in claim 38, “a trench formed in a substrate on at least a portion of a periphery of the active area of the integrated circuit, wherein the trench extends to a surface of a base layer below the substrate, and wherein the trench has sidewalls and the trench includes a top width and a base layer width where the base layer width is smaller than the top width; an insulating liner formed along the sidewalls; and a first fill material formed over the insulating liner that at least partially fills the trench and prevents at least a portion of photons or electrons from passing through the trench”;

in claim 44, “at least one trench extending from the surface of the substrate into the substrate to a depth of at least about 0.5 μ m and with a length extending across the surface of the substrate between the source area and the active area and the at least

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one trench includes a top width and a base layer width where the base layer width is smaller than the top width”;

in claim 45, “at least one trench around at least a portion of the array, wherein the trench extends from the surface of the substrate to a depth of at least about 0.5 μ m into the substrate and the at least one trench includes a top width and a base layer width where the base layer width is smaller than the top width wherein the at least one trench structure has sidewalls and contains a first material that prevents a portion of photons or charged particles from passing through the trench structure to the array”;

in claim 46, “an integrated circuit coupled to the processor, the integrated circuit comprising a structure for isolating an active area on the integrated circuit, the structure comprising: a trench extending from a surface of a substrate to a depth of at least about 0.5 μ m into the substrate and the trench includes a top width and a base layer width where the base layer width is smaller than the top width”;

in claim 69, “the trench extends from the surface to the lower layer, prevents at least a portion of photons or charged particles from passing through the trench structure to the array; has sidewalls and contains a first material that prevents at least a portion of photons or charged particles from passing through the trench structure to the array; and contains a second material that partially fills the trench structure, wherein the second material prevents at least a portion of photons or charged particles from passing through the trench structure to the array”;

in claim 73, “a trench formed in a substrate of the integrated circuit along at least a portion of a periphery of the active area, the substrate having a lower layer and an

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upper layer on the lower layer, wherein the trench extends from a surface of the upper layer to a surface of the lower layer; an insulating liner formed along sidewalls of the trench; a first fill material formed over the insulating liner wherein the first fill material at least partially fills the trench and prevents at least a portion of photons and electrons from passing through the trench to the active area, and a second fill material that partially fills the trench, wherein the second material prevents at least a portion of photons from passing through the trench”;

in claim 77, “a plurality of trenches formed in a substrate of the integrated circuit on at least a portion of a periphery of the active area, wherein a depth of each of the plurality of trenches extends to a surface of a base layer of said substrate and the plurality of trenches include a first fill material that at least partially fills each of the plurality of trenches and prevents at least a portion of photons or charged particles from passing through the trench wherein the first fill material is a high extinction coefficient material”; and

in claim 78, “a plurality of trenches formed in a substrate of the integrated circuit on at least a portion of a periphery of the active area, wherein a depth of each of the plurality of trenches extends to a surface of a base layer of said substrate and the plurality of trenches include: a first fill material that at least partially fills each of the plurality of trenches and prevents at least a portion of photons or charged particles from passing through the trench; and a second fill material that partially fills each of the plurality of trenches, wherein the second material prevents at least a portion of photons from passing through the trench”.

The dependent claims being further limiting and definite are also allowable.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patents are cited to further show the state of the art with respect to integrated circuit trench structures:

Chen et al. (6,118,142)	Lee et al. (5,535,231)
Nakagawa et al. (5,838,174)	Radford et al. (5,721,429)
Rogers et al. (US 6,707,075 B1)	Scales et al. (US 2004/0173865 A1)
Tani et al. (US 6,580,095 B2).	

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ida M. Soward whose telephone number is 571-272-1845. The examiner can normally be reached on Monday - Thursday 6:30am to 5:00pm.

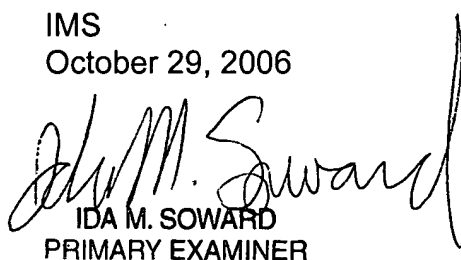
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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra V. Smith can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

IMS

October 29, 2006



IDA M. SOWARD
PRIMARY EXAMINER